Advanced Analog Integrated Circuits

Device Models

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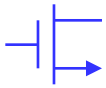


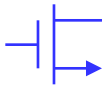
The Problem With MOS Transistor Models

Square laws

→ simple

→ V_{th}, μC_{ox}, λ

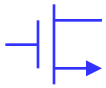
ASIC



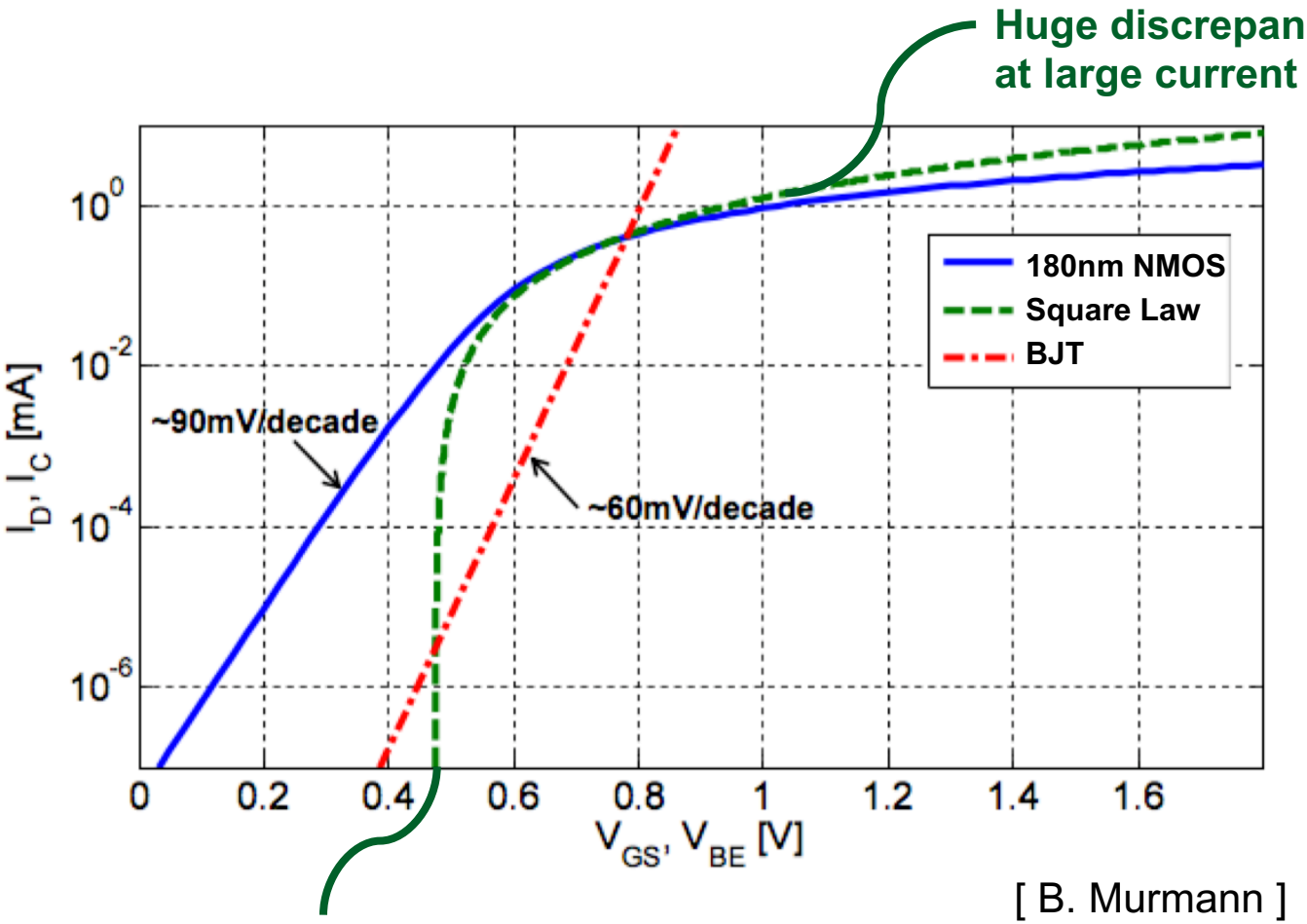
Simulator Models (BSIM, …)

180nm NMOS model parameters:

```
1: type=n lmin=0.18e-6  lmax=0.501e-6   wmin=0.4e-6  wmax=10.001e-6.
+ minr=1e-60 tnom=25 version=3.1 tox=toxn xj=1.6e-7 nch=3.9e+17 .
+ lln=1 lwn=1 wln=1 wwn=1 lint=1e-8 ll=0 lw=0 lwl=0 wint=1e-8 wl=0 ww=0 wwl=0 .
+ mobmod=1 binunit=2 xl=-2e-8 + dlxn xw=0 + dxwn dwg=0 dwb=0 ldif=9e-8 .
+ hdif=hdifn rsh=6.8 rd=0 rs=0 vth0=0.48 + dvthn lvth0=1.18e-8 wvth0=-7.08e-9 .
+ pvth0=-3.07e-15 k1=0.49 lk1=4.82e-8 wk1=-1.67e-8 pk1=-4.58e-15 .
+ k2=0.03 lk2=-2.01e-8 wk2=6.03e-10 pk2=5.87e-16 k3=0 dvt0=0 dvt1=0 .
+ dvt2=0 dvt0w=0 dvt1w=0 dvt2w=0 nlx=0 w0=0 k3b=0 vsat=84638 lvsat=-0.0002 .
+ wvsat=0.001 pvsat=1.71e-11 ua=-5.07e-10 lua=-5.58e-17 wua=-4.34e-17 .
+ pua=2.42e-23 ub=1.98e-18 lub=4.99e-26 wub=-2.70e-26 pub=-5.53e-32 .
+ uc=7.19e-11 luc=1.46e-17 wuc=-3.71e-19 puc=-1.43e-23 rdsw=170 .
+ prwb=0 prwg=0 wr=1 u0=0.04 lu0=5.93e-10 wu0=-5.39e-10 pu0=5.68e-16 .
+ a0=0.54 la0=7.71e-8 wa0=1.31e-7 pa0=-6.57e-14 keta=-0.027 .
+ lketa=1.75e-9 wketa=2.62e-9 pketa=-9.24e-16 a1=0 a2=0.99 ags=0.039.
+ lags=-8.58e-9 wags=-1.49e-9 pags=6.84e-16 b0=0 b1=0 voff=-0.13.
+ lvoff=1.25e-10 wvoff=5.07e-9 pvoff=-2.82e-15 nfactor=1 cit=0.0002.
+ lcit=1.32e-10 wcit=4.29e-11 pcit=-1.97e-17 cdsc=0 cdscb=0 cdscd=0 eta0=-0.0003
+ leta0=1.93e-10 weta0=3.35e-11 peta0=-1.54e-17 etab=0.0014 letab=-6.99e-10 .
+ wetab=-4.11e-11 petab=1.89e-17 dsub=0 pclm=0.97 lpclm=7.37e-8 .
+ wpclm=2.16e-7 ppclm=-1.59e-15 pdiblc1=1e-6 pdiblc2=-0.0035 lpdiblc2=4.38e-9 .
+ wpdiblc2=-1.24e-9 ppdiblc2=5.71e-16 pdiblcb=0.01 drout=0 pscbe1=4e+08 .
+ pscbe2=1e-6 pvag=0 delta=0.01 alpha0=6.27e-8 beta0=11.60 kt1=-0.23.
+ lkt1=1.96e-9 wkt1=1.35e-9 pkt1=1.97e-15 kt2=-0.027 lkt2=-3.83e-10 .
+ wkt2=-5.19e-9 pkt2=1.23e-15 at=20000 ute=-1.09 lute=-6.90e-8 .
```



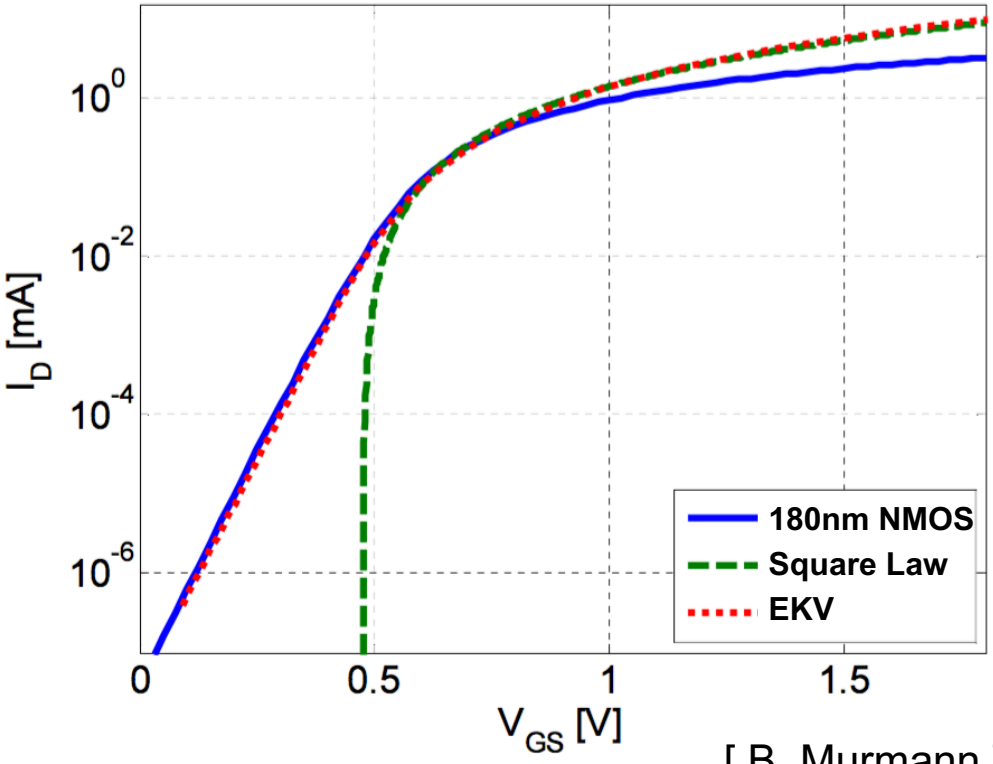
Square Law Model



[B. Murmann]

Middle of the Road: EKV Model

C. Enz and E. A.Vittoz, *Charge-Based MOS Transistor Modeling - The EKV Model for Low-Power and RF IC Design,* Wiley, 2006.



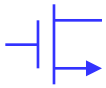
[B. Murmann]

In saturation region:

$$I_D = 2nV_t^2 \cdot \mu C_{ox} \frac{W}{L}(q_s^2 + q_s)$$

$$V_{GS} - V_{TH} = nV_t[2(q_s - 1) + \ln(q_s)]$$

- Only 3 parameters: V_{TH}, n, $\mu C_{ox} \frac{W}{L}$ (functions of L, …)
- Parametric in q_s, normalized source charge density
- Good agreement except at high I_D
- Still impractical for hand calculations



Designer's Wish list

1) Accurately model reality
   - e.g. BSIM, PSP
2) "Model" simple ← for hand calcs.

240B Approach

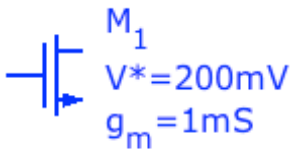
1) Linear
   - → speed (BW, t_s)
   - → DR
   - → Power dissipation

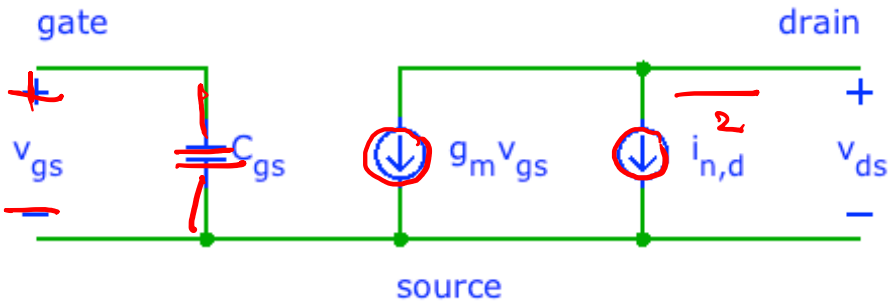
2) Refinements
   - → a_{vo}

3) W, L

4) Verify. Iterate

Basic Transistor Model for Design





$$\overline{i_{n,d}^2} = 4kT \cdot \gamma \cdot g_m \cdot \Delta f$$

$$= 4kT \cdot \frac{1}{\eta R_{eq}} \cdot \Delta f$$

$0.5 \ldots 1$

Transistor FOMs

1) Current efficiency

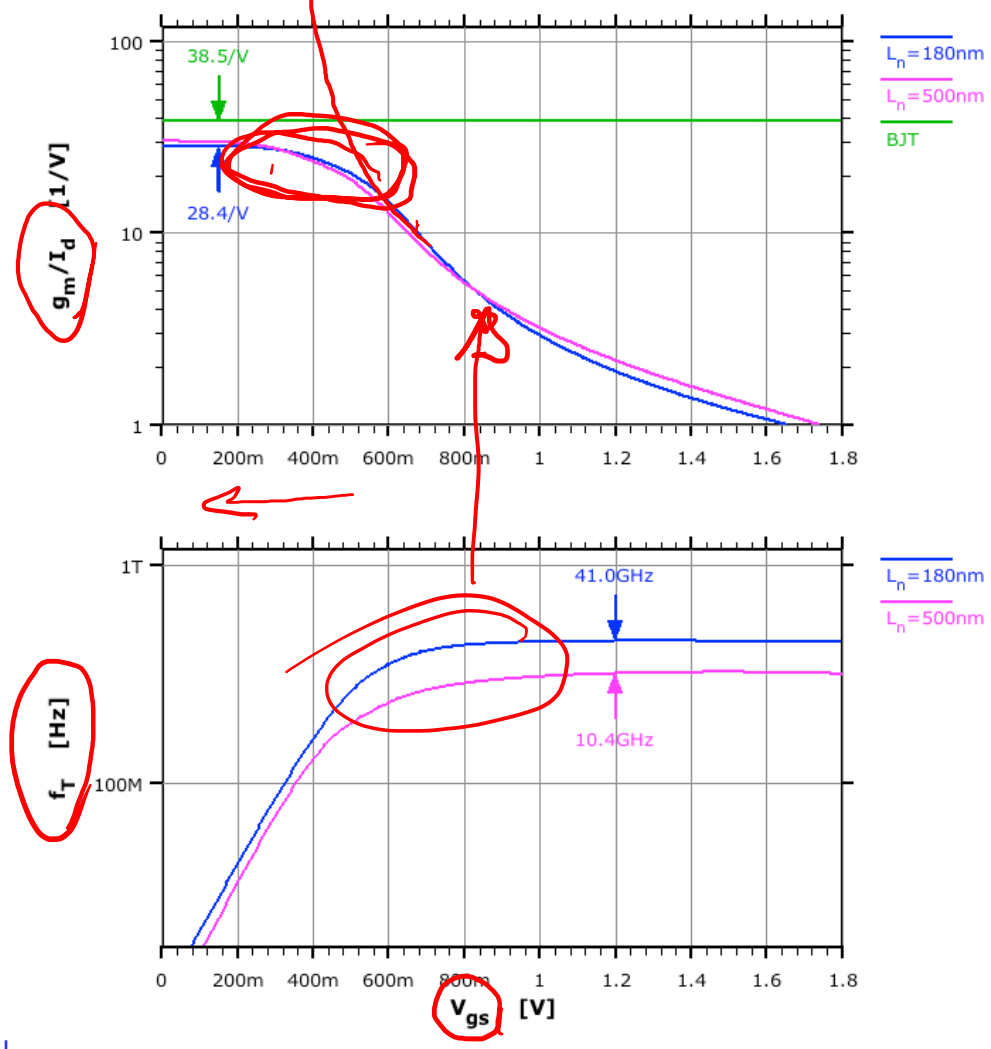
$$\frac{g_m}{I_D} = \frac{2}{V^*}$$

$$V^* = \frac{2 I_D}{g_m}$$

2) Cutoff freq

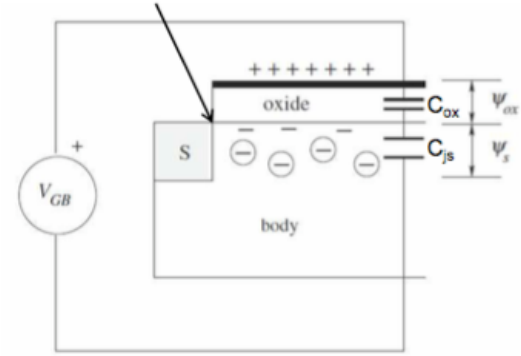
$$f_T = \frac{1}{2\pi} \cdot \frac{g_m}{C_{GS}}$$

FOMs for 180nm Process

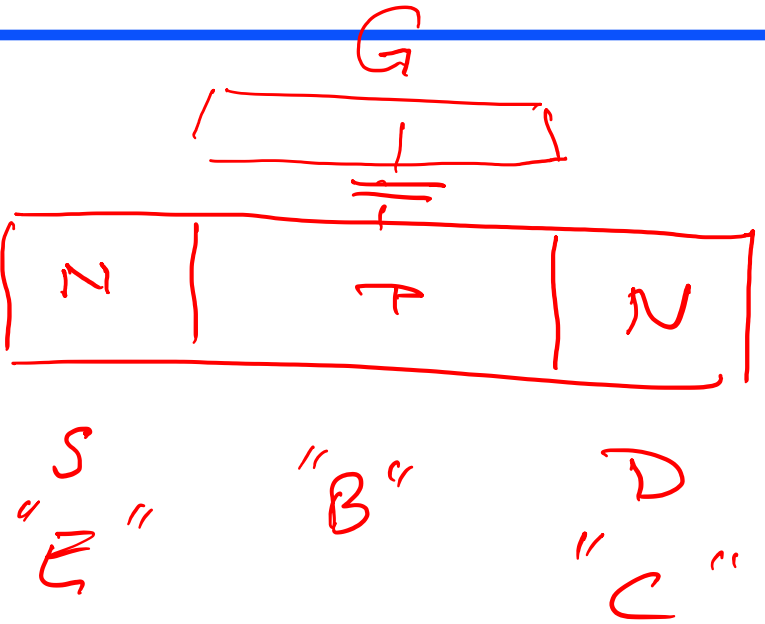


Subthreshold Conduction (Weak Inversion)

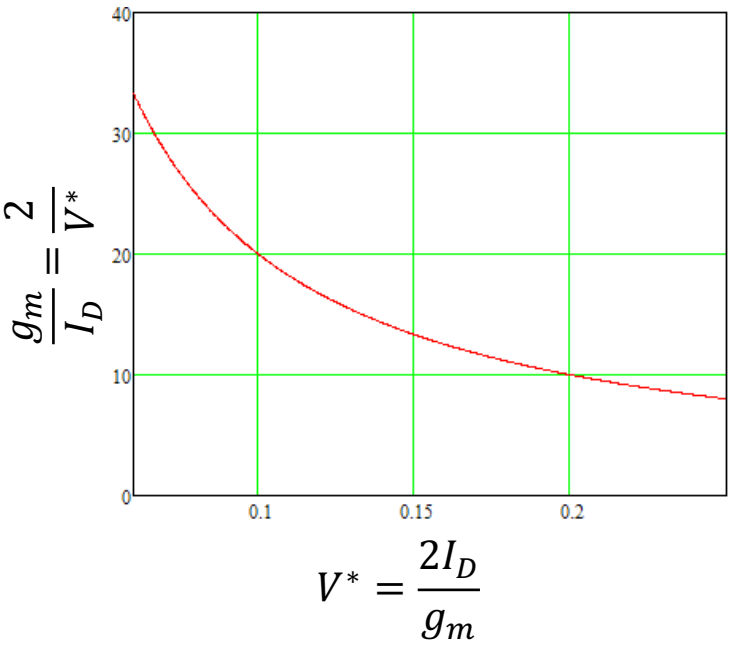
Channel potential is higher than source → forward bias



D.L. Pulfrey, Understanding Modern Transistors and Diodes, Cambridge University Press, 2010.

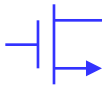


g_m/I_D or V^*

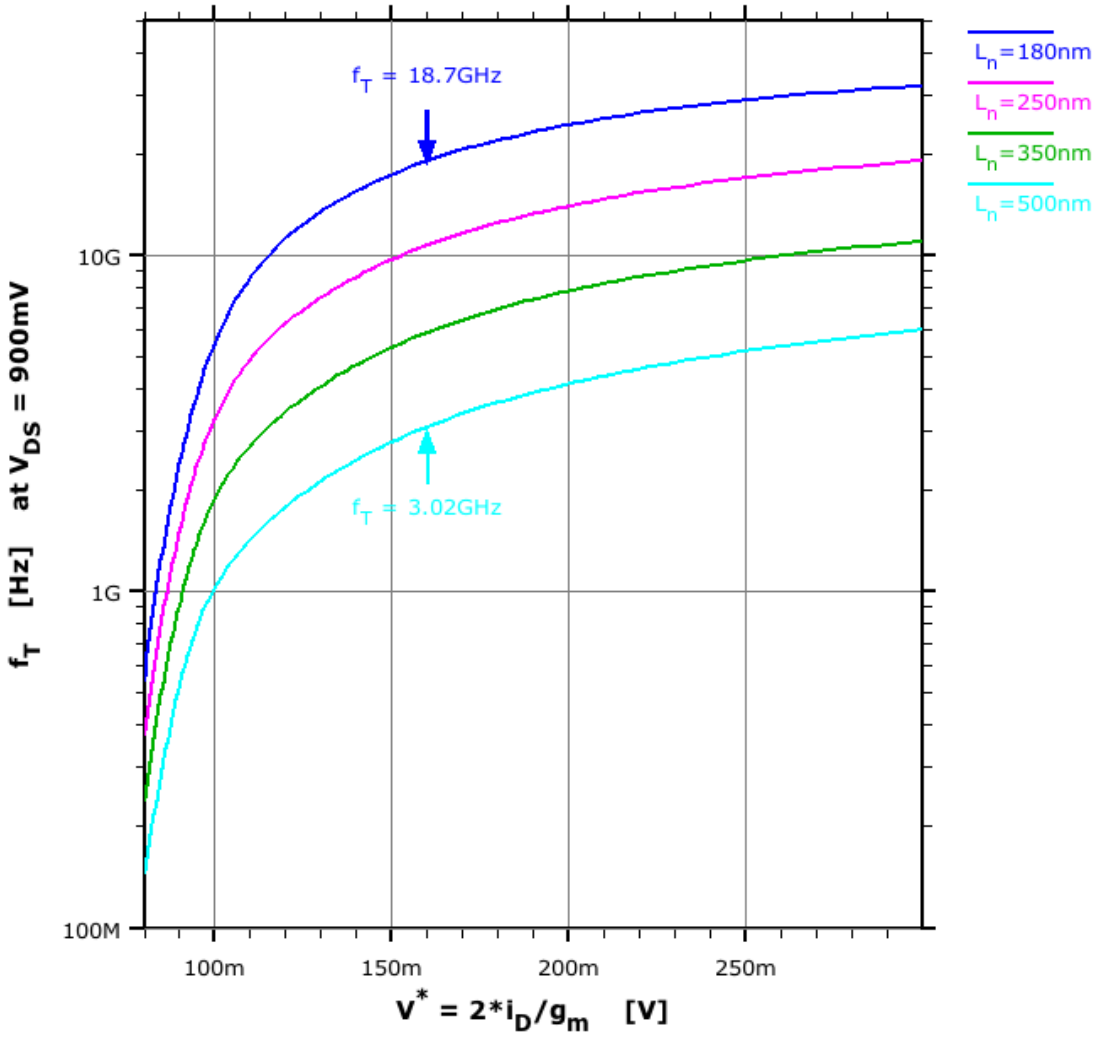


$\frac{g_m}{I_D}$ [1/V]	V^* [mV]
38.5	$2V_t$ = 52
30	67
25	80
20	100
16	125
12.5	160
10	200

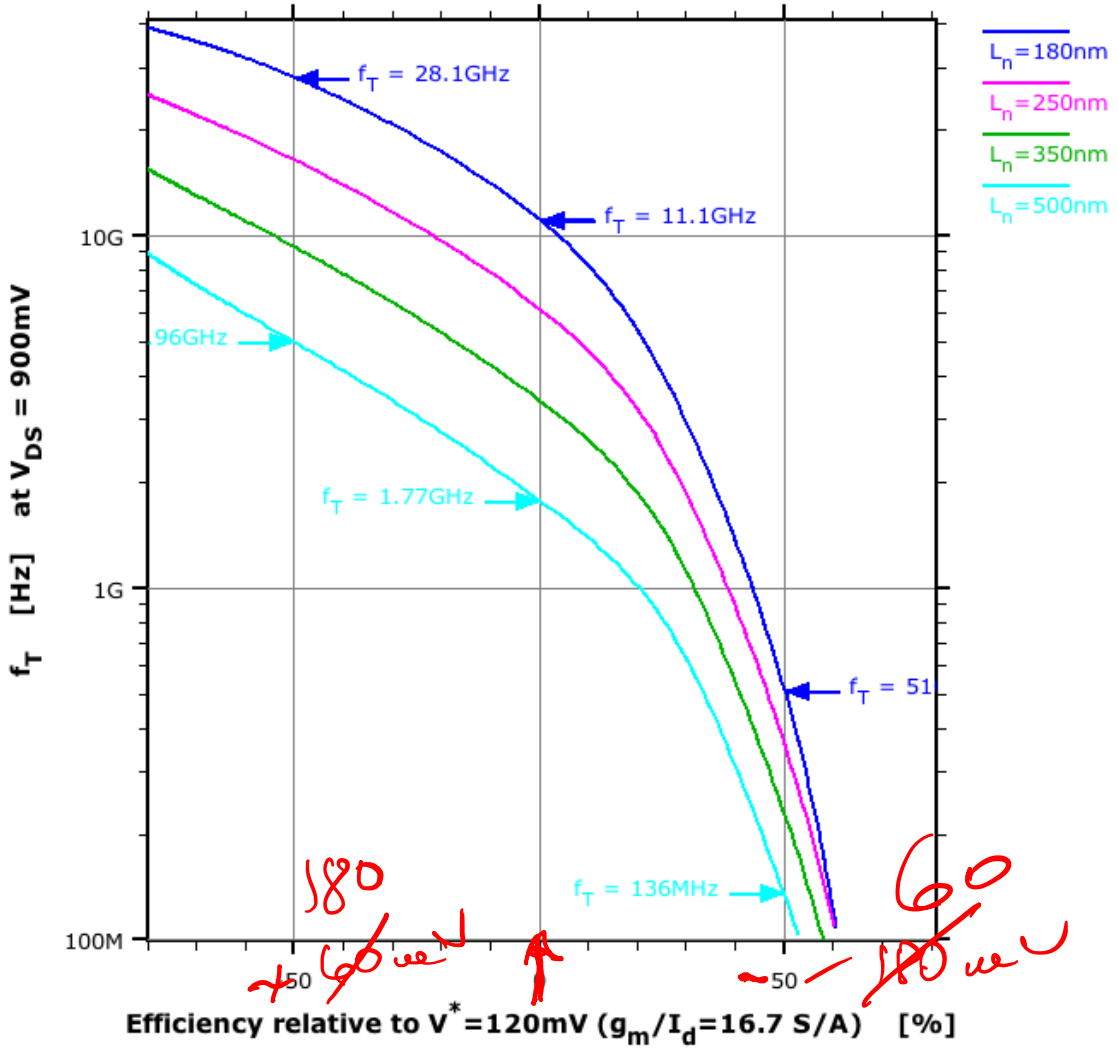
Interchangeable, use whichever you prefer



f_T versus V^* (not V_{GS})



Relative Power Efficiency



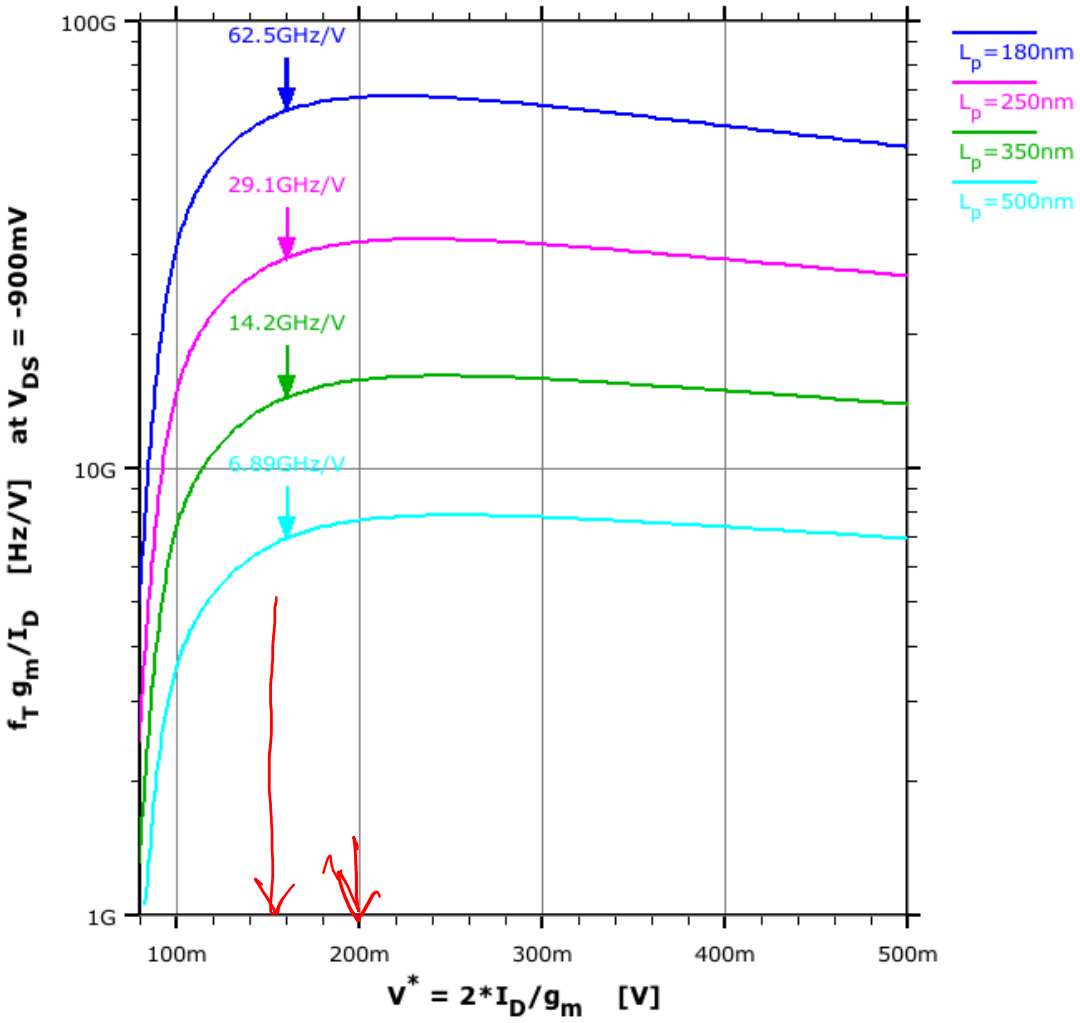
Same data, but horizontal axis shows current efficiency relative to $V^* = 120\text{mV}$ $\left(\frac{g_m}{I_d} = 16.7\ \text{S/A}\right)$.

For the 180nm device, the f_T decreases by more than 20x when V^* is lowered to 80mV for a 50% higher current efficiency.

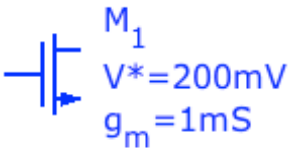
Increasing V^* to 180mV decreases the current efficiency by 50% but boosts f_T only by a factor 2.5.

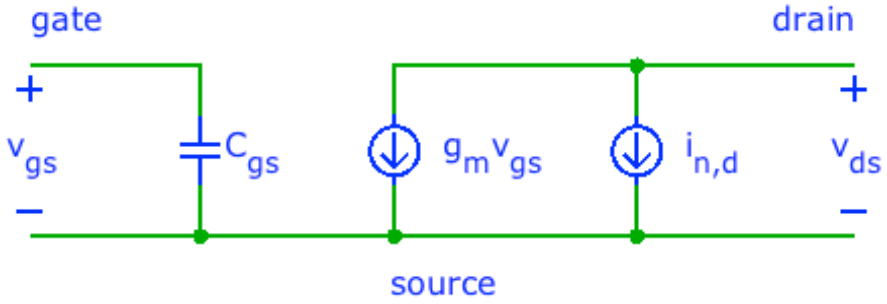
Devices are rarely operated with V^* outside the range 80mV … 200mV.

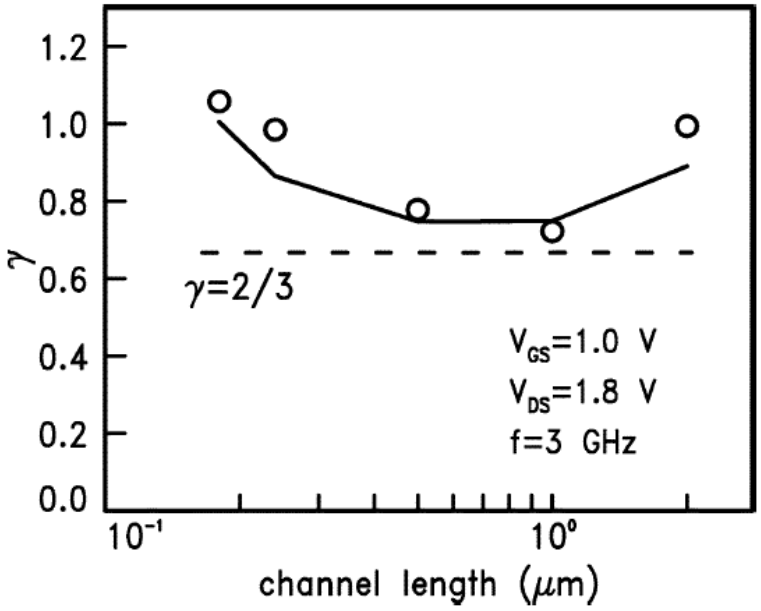
Composite $FOM = f_T \cdot \frac{g_m}{I_D}$



Noise Model

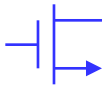




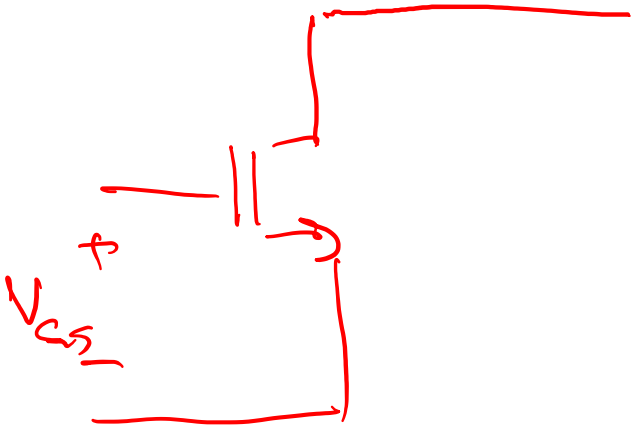


$$\overline{i_{n,d}^2} = 4k_B T \frac{\gamma}{g_{m-1}} \Delta f$$

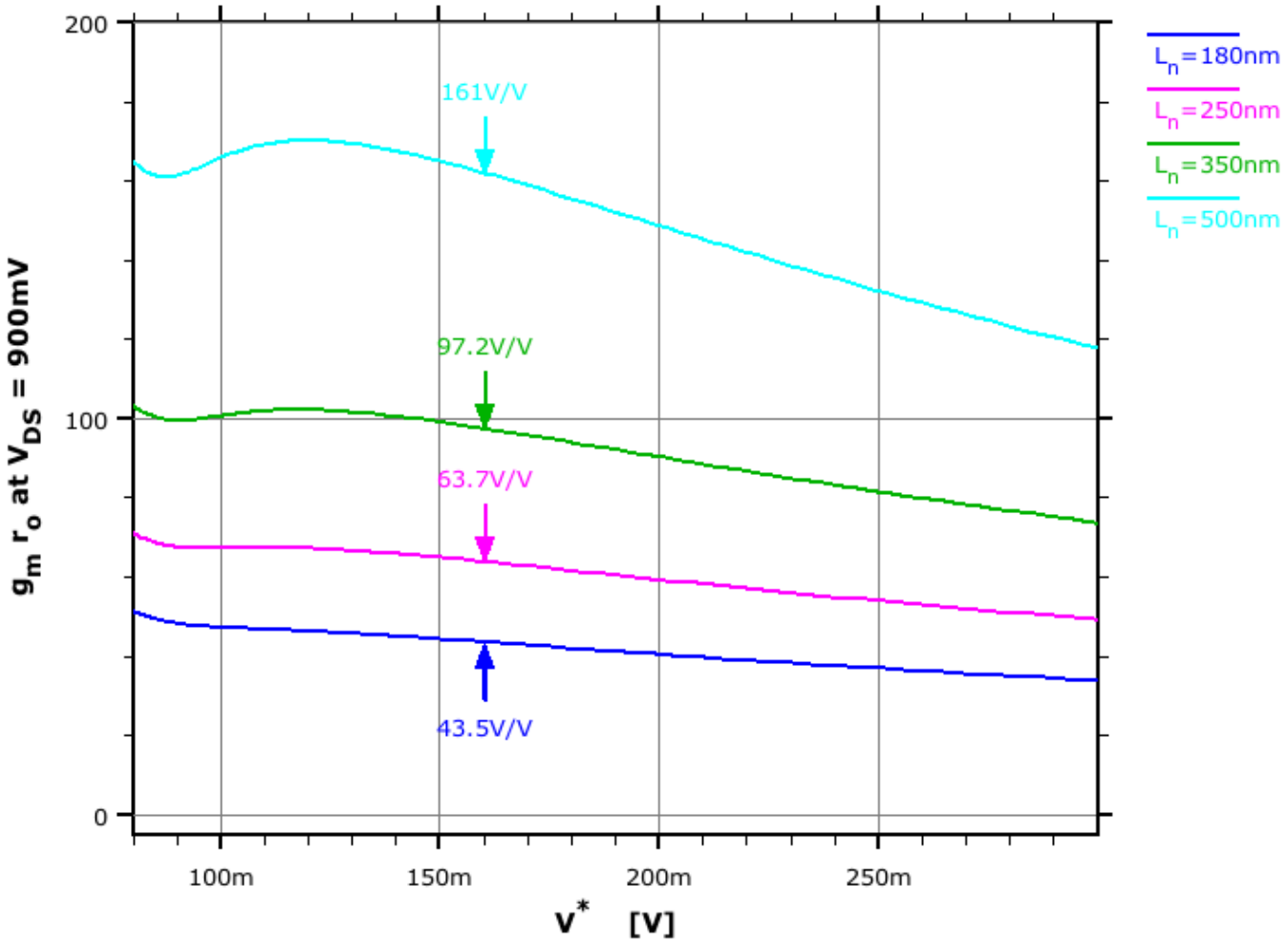
A. J. Scholten et al., "Noise modeling for RF CMOS circuit simulation," IEEE Trans. Electron Dev., pp. 618-632, Mar. 2003.



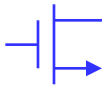
Extracting γ with Simulator



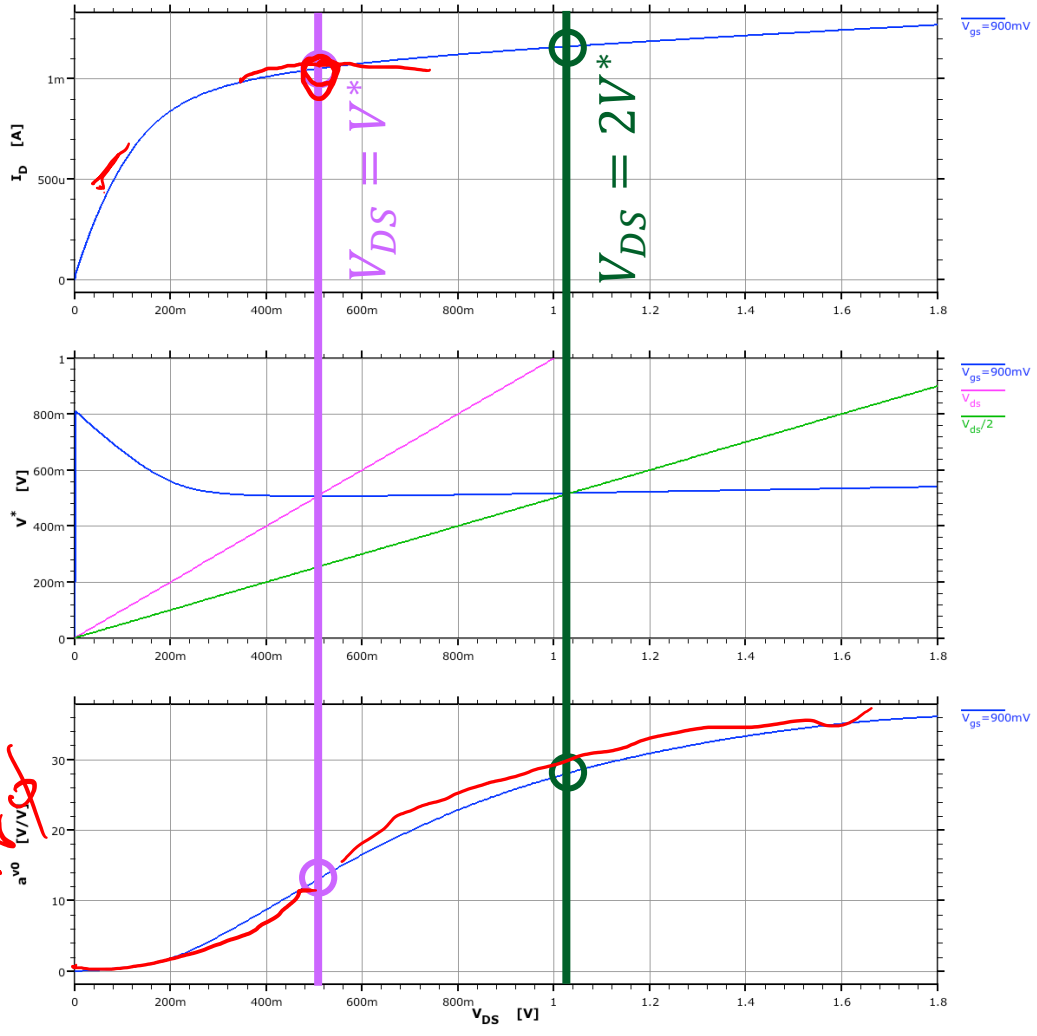
Intrinsic Gain $A_{v0} = g_m \cdot r_o$



“Saturation”



a_v versus V_{DS}



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Extrinsic Elements

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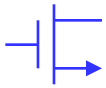
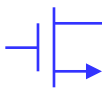


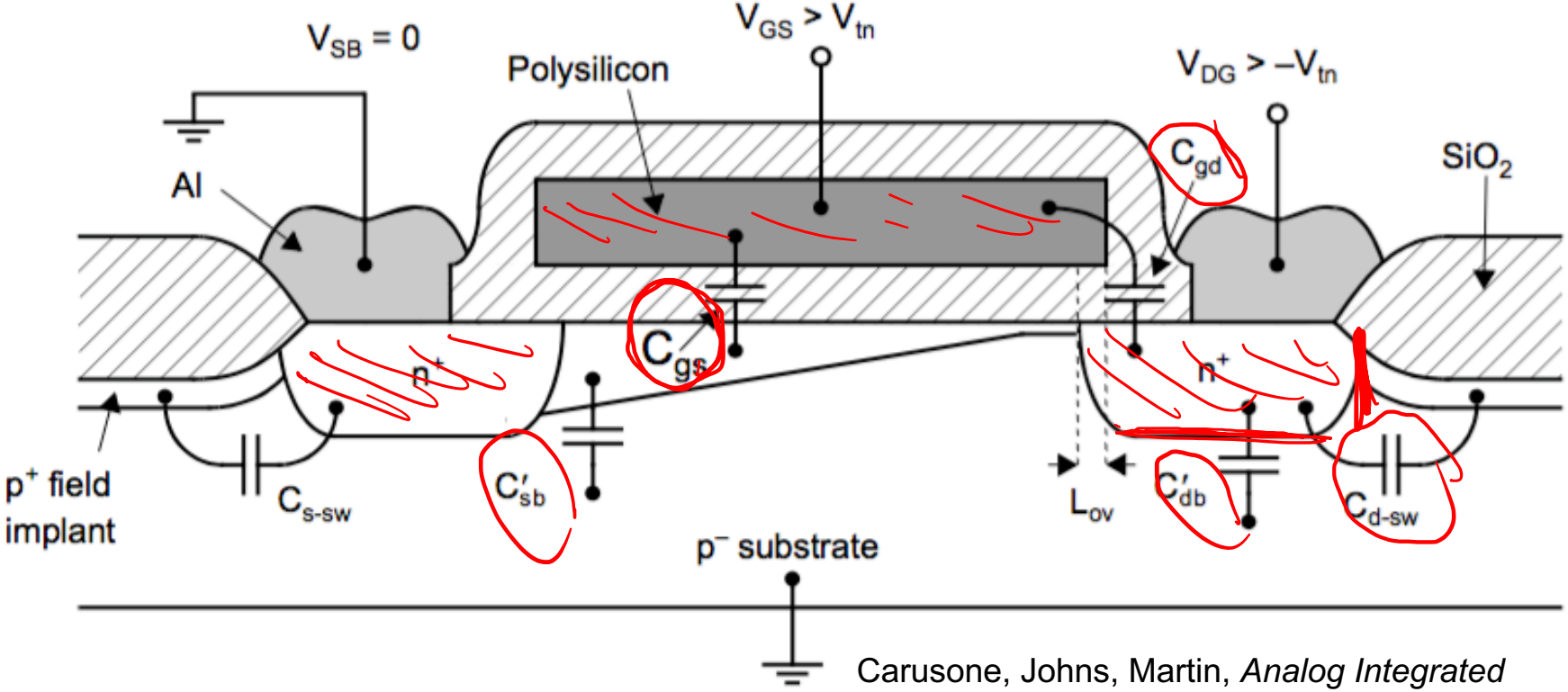
Extrinsic Circuit Elements

* Basic model : g_m, C_{GS}, $\overline{i_{dn}^2}$

* Real XTRs:
  - → Extr. caps C_{SB}, ---
  - → Lead resistance
  - → Add noise source
    - * Flicker, 1/f noise
    - * Lead resistance
  - → Body effect



MOS Capacitances



Carusone, Johns, Martin, *Analog Integrated Circuit Design,* 2nd Edition, Wiley, 2011, p. 31.

$$C_{db} = \frac{AD\,C_J}{\left(1+\frac{V_{DB}}{PB}\right)^{MJ}} + \frac{PD\,C_{JSW}}{\left(1+\frac{V_{DB}}{PB}\right)^{MJSW}}$$

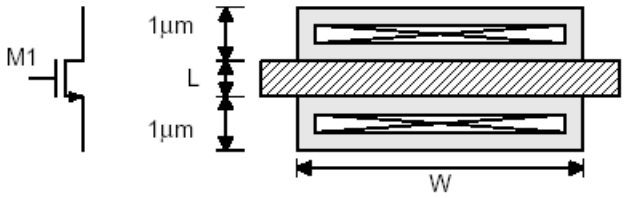
$$AD = WL_{diff}$$

$$PD = W + 2L_{diff}$$

Get parameters from technology file

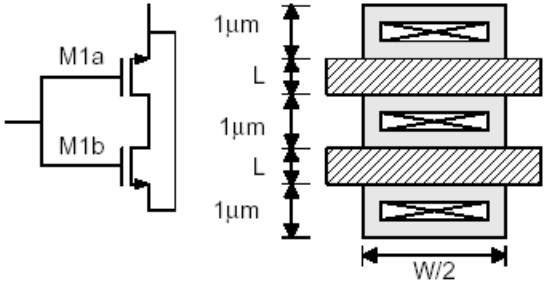
Source and Drain Junctions – Layout

Individual devices:

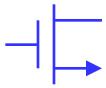


AS = AD =1µm * W
PS = PD = 2µm + W
e.g. NMOS, W=20µm, V_{sb}=0V
$C_{sb} = C_{db}$ = 28fF

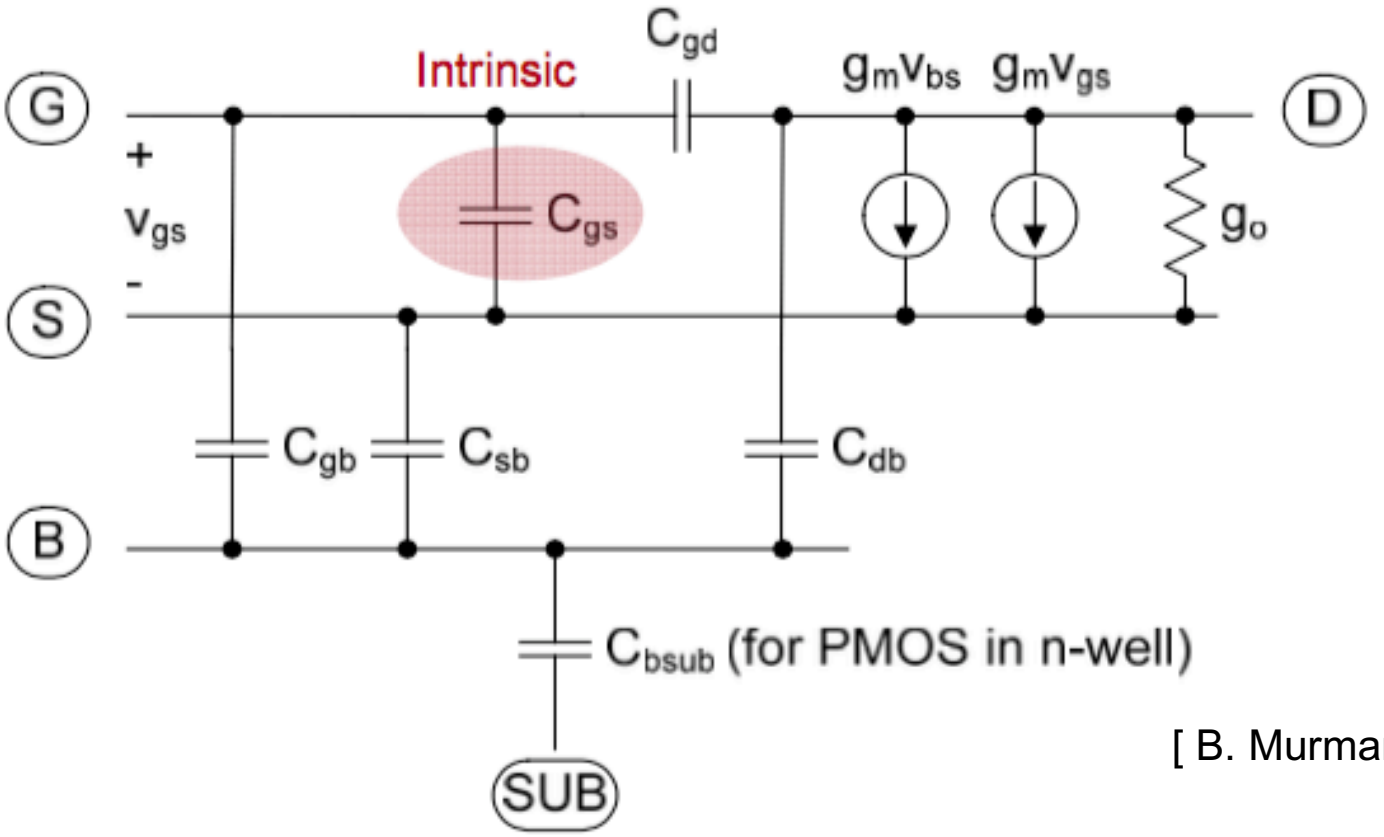
Wide devices consisting of multiple individual ones wired in parallel:



AS = 1µm * W
PS = 4µm + W
AD = 1µm * W/2
PD = 2µm
e.g. NMOS, W=20µm, V_{sb}=0V
C_{sb} = 29fF
C_{db} = 10fF

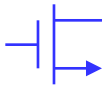


Complete Small Signal Model



[B. Murmann]

$$C_{gg} = C_{gs} + C_{gb} + C_{gd} \qquad C_{dd} = C_{db} + C_{gd}$$

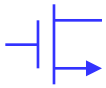


Gate Capacitance Summary

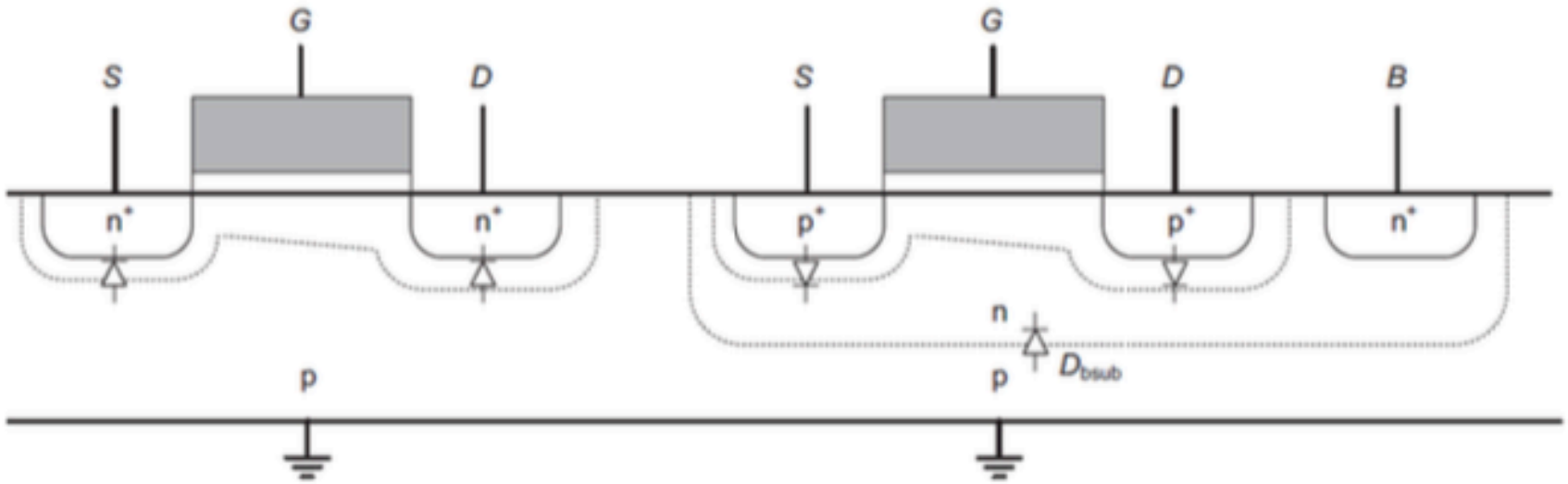
	Subthreshold	Triode	Saturation
C_{GS}	C_{ol}	$C_{GC}/2 + C_{ol}$	$2/3\ C_{GC} + C_{ol}$
C_{GD}	C_{ol}	$C_{GC}/2 + C_{ol}$	C_{ol}
C_{GB}	C_{GC} // C_{CB}	0	0

$$C_{GC} = WLC_{ox} \qquad C_{ol} = WC'_{ol}$$

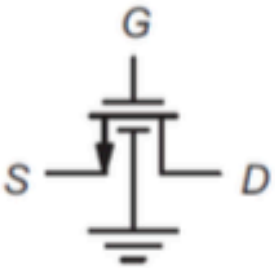
$$C_{CB} = \frac{1}{C_{js}}$$

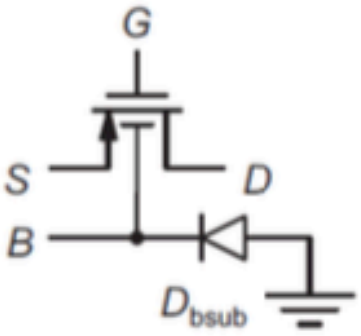


Well Capacitance



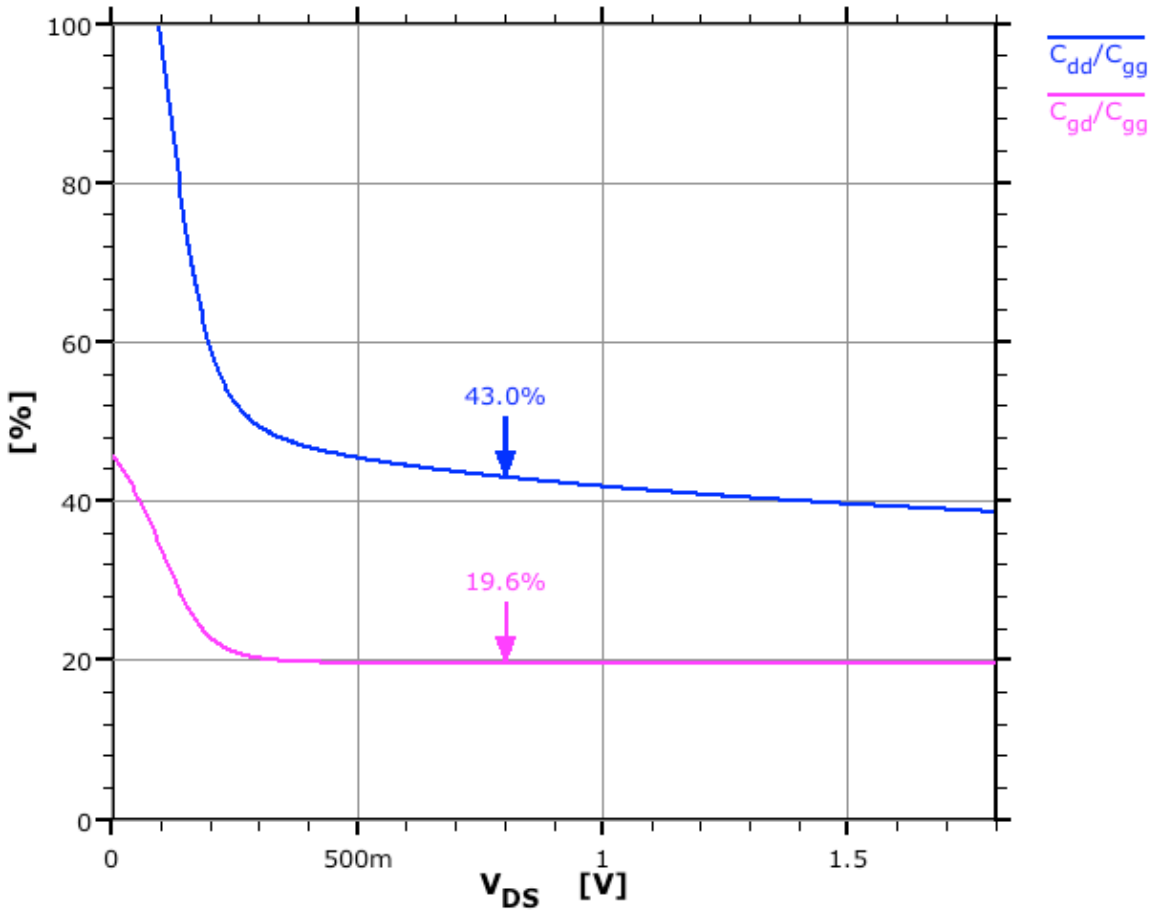
[B. Murmann]



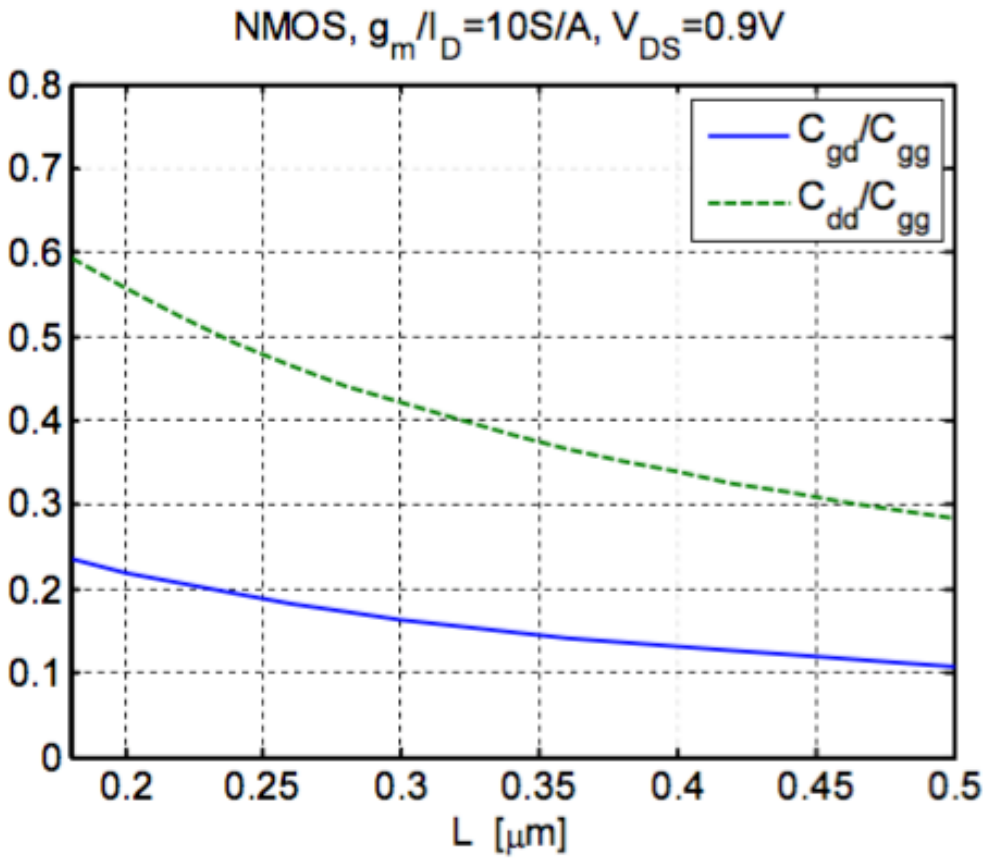


D_{bsub} not part of 4-terminal SPICE transistor model!

Extrinsic Capacitances



Extrinsic Capacitance versus L



[B. Murmann]

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Design Flow

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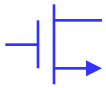


Generic Design Flow

1) g_m $\quad V^* \triangleq \frac{2}{g_m/I_D}$

2) Pick L →
   long → high A_{VO}
   short → high f_T

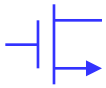
3) V^* low → high $\frac{g_m}{I_D}$, low power
   high → " f_T

4) $I_D = \frac{g_m}{g_m/I_D}$ $\quad C_{GS}$ $\quad f_T \approx \frac{1}{2\pi}\frac{g_m}{C_{GS}}$

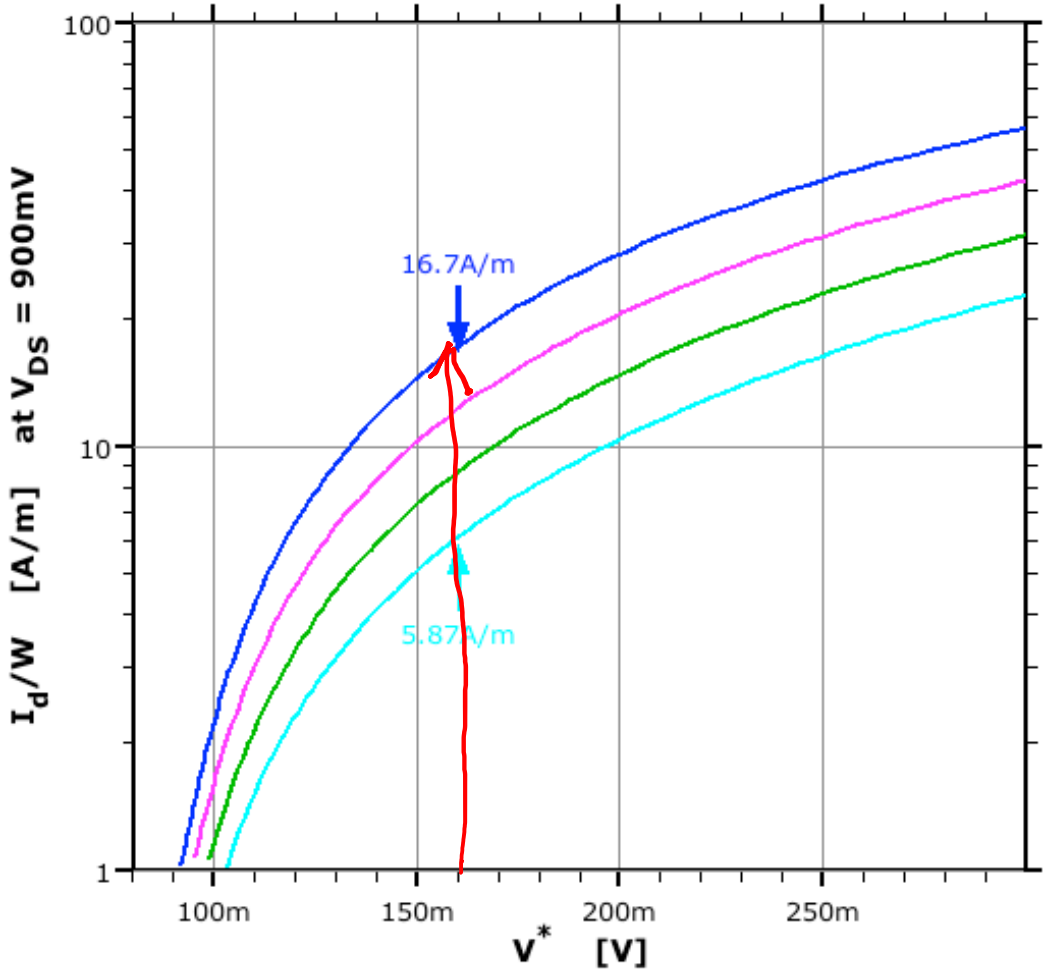
5) Verify!

6) W

7) Verify



Current Density → W



$I_D/W = 16.7\ A/m$

$I_D = 80\mu A$

$W = \dfrac{I_D}{I_D/W} = 4.8\ \mu m$